CLAIMS

What is claimed is:

1. An under bump metallization structure applicable to be disposed on bonding pads of a semiconductor wafer, wherein a passivation layer covers the wafer and exposes the bonding pads, the under bump metallization structure comprising:

   an adhesive layer formed on the bonding pads;

   a first barrier layer disposed on the adhesive layer;

   a wetting layer formed on the first barrier layer; and

   a second barrier layer disposed on the wetting layer, wherein a material of the second barrier comprises lead.

2. The structure of claim 1, wherein the material of the second barrier layer is made of lead and tin.

3. The structure of claim 2, wherein the ratio of the lead and the tin in weight is substantially ninety-five to five.

4. The structure of claim 2, wherein the ratio of the lead and the tin in weight is substantially ninety-seven to three.

5. The structure of claim 2, wherein the ratio of the lead and the tin in weight is substantially ninety to ten.

6. The structure of claim 1, wherein the first barrier layer is a nickel-vanadium layer.

7. The structure of claim 1, wherein the wetting layer is a copper layer.

8. The structure of claim 1, wherein the wetting layer is a nickel layer.

9. The structure of claim 1, wherein the wetting layer is a titanium layer.

10. The structure of claim 1, wherein the thickness of the second barrier layer is ranged from about 50 μm to about 80 μm.

11. A semiconductor wafer applicable to a flip chip device, comprising:

an active surface;

a plurality of bonding pads formed on the active surface;

a passivation covering the active surface and exposing the bonding pads;

a first electrically conductive layer formed on the bonding pads; and

a second electrically conductive layer formed on the first electrically conductive layer, wherein a material of the second electrically conductive layer comprises lead.

12. The semiconductor wafer of claim 11, further comprising a plurality of bumps formed above the bonding pads and attached to the second electrically conductive layer.

13. The semiconductor wafer of claim 11, wherein the second electrically conductive layer is extended above the active surface.

14. The semiconductor wafer of claim 11, further comprising a dielectric layer covering the second electrically conductive layer and exposing a portion of the second electrically conductive layer to form a redistributed pad.

15. The semiconductor wafer of claim 14, further comprising a bump formed on the redistributed pad.

16. The semiconductor wafer of claim 11, wherein a material of the first electrically conductive layer is selected from the group of aluminum, titanium,

titanium-vanadium alloy, titanium-tungsten alloy, copper, nickel-copper alloy, and nickel, nickel-vanadium alloy.

17. The semiconductor wafer of claim 11, wherein the second electrically conductive layer is a lead-tin layer.

18. The semiconductor wafer of claim 11, wherein the first electrically conductive layer comprises a titanium layer, an aluminum layer, a nickel-vanadium alloy layer and a copper layer and the titanium layer is directly attached to the bonding pads.

19. The semiconductor wafer of claim 11, wherein a material of the dielectric layer comprises polyimide.

20. The semiconductor wafer of claim 11, wherein the material of the second electrically conductive layer is made of lead and tin, and the ratio of the lead and the tin in weight is substantially ninety-five to five, ninety-seven to three or ninety to ten.

21. The semiconductor wafer of claim 17, wherein the thickness of the lead-tin layer is at least larger than 50μm.